Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for observing the state of internal signals during chip testing, comprising:

receiving specific test signals by a plurality of multiplexers in at least one module ~~in order to form a plurality of test signal groups~~;

combining, by the plurality of multiplexers, ~~the specific~~ test signals received for each test signal group to create a [[the]] plurality of test signal groups;

receiving, by mapping logic, one of said plurality of test signal groups from each one of said plurality of multiplexers; and

mapping, by said mapping logic, one of said plurality of test signal groups to any one of a plurality of outputs of said mapping logic to output as a test output group.

~~identifying specific test signal groups in order to form a plurality of test signal output groups; and~~

~~mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups.~~

2. (Original) The method of claim 1 wherein the at least one module includes a plurality of modules.

3. (Original) The method of claim 2, further comprising:

concurrently observing test signals for a plurality of modules.

4. (Original) The method of claim 3 wherein the plurality of modules includes identical modules.

5. (Currently amended) The method of claim 1 further comprising:

said mapping logic including a plurality of mapping multiplexers;

each one of said plurality of mapping multiplexers receiving said plurality of test signal groups;

each one of said plurality of mapping multiplexers generating a different one of said plurality of outputs of said mapping logic; and

each one of said plurality of mapping multiplexers selecting one of said plurality of test signal groups to output as a test output group.

~~wherein combining the specific test signals received for each test signal group to create the plurality of test signal groups is performed by a multiplexer.~~

6. (Currently amended) The method of claim 1 wherein said mapping logic is ~~mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups is performed using~~ byte lane mapping logic.

7. (Canceled)

8. (Currently amended) A system for observing the state of internal signals during chip testing, comprising:

means for receiving specific test signals by a plurality of multiplexers in at least one module ~~in order to form a plurality of test signal groups~~;

the plurality of multiplexers ~~means for~~ combining the specific test signals received for each test signal group to create a [[the]] plurality of test signal groups;

mapping logic for receiving one of said plurality of test signal groups from each one of said plurality of multiplexers; and

said mapping logic mapping one of said plurality of test signal groups to any one of a plurality of outputs of said mapping logic to output as a test output group.

~~means for identifying specific test signal groups in order to form a plurality of test signal output groups; and~~

~~means for mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups.~~

9. (Original) The system of claim 8 wherein the at least one module includes a plurality of modules.

10. (Original) The system of claim 9, further comprising:
concurrently observing test signals for a plurality of modules.

11. (Original) The system of claim 10 wherein the plurality of modules includes identical modules.

12. (Currently Amended) The system of claim 8 further comprising:
said mapping logic including a plurality of mapping multiplexers;
each one of said plurality of mapping multiplexers receiving said plurality of test signal groups;

each one of said plurality of mapping multiplexers generating a different one of said plurality of outputs of said mapping logic; and

each one of said plurality of mapping multiplexers selecting one of said plurality of test signal groups to output as a test output group.

~~wherein the means for combining the specific test signals received for each test signal group to create the plurality of test signal groups is a multiplexer.~~

13. (Currently amended) The system of claim 8 wherein the mapping logic is ~~means for mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups is performed using~~ byte lane mapping logic.

14. (New): The method according to claim 1, further comprising:

mapping, by said mapping logic, a first one of said plurality of test signal groups, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first test output group;

mapping, by said mapping logic, a second one of said plurality of test signal groups, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second test output group; and

said first one of said plurality of test signal groups and said second one of said plurality of test signal groups being a same signal type of signal.

15. (New): The system according to claim 8, further comprising:

said mapping logic mapping a first one of said plurality of test signal groups, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first test output group;

said mapping logic mapping a second one of said plurality of test signal groups, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second test output group; and

said first one of said plurality of test signal groups and said second one of said plurality of test signal groups being a same signal type of signal.